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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,727	03/08/2004	Jeffrey R. Jobs	33585/US	3937

27076 7590 04/13/2007

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EXAMINER	
PATEL, HETUL B	
ART UNIT	**PAPER NUMBER**
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/797,727	JOBS ET AL.	
	Examiner	Art Unit	
	Hetul Patel	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-17,19-44,46,47 and 49-122* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-17,19-44,46,47 and 49-122* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/16/06,12/26/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to the amendment filed on December 26, 2006. This amendment has been entered and carefully considered. Claims 2, 18, 45 and 48 were previously cancelled; claims 15, 22, 33, 49-52, 64, 71, 76, 80, 90, 96 and 101 are amended. Therefore, claims 1, 3-17, 19-44, 46-47 and 49-122 are pending in the current application.

2. The claim objection and the rejection under 35 USC 112, first paragraph, made in the previous office action have been withdrawn due to the amendment filed on December 26, 2006.

3. Applicant's arguments filed on December 26, 2006 have been considered but are moot in view of the new ground(s) of rejection.

Information Disclosure Statement

4. The information disclosure statements (IDS) submitted on 10/16/2006 and 12/26/2006 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the examiner.

Drawings

5. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid

abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3-12, 15-17, 19-30, 33-44, 46-47, 49-61, 64-68, 71-73, 76-78, 80-87, 90-93, 96-99 and 101-122 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art hereinafter AAPA in view of Zhu (Pat No 5,423,009).

As per claim 1, AAPA teaches that in a memory system (i.e. 100 in Fig. 1) having a memory hub controller (i.e. 128 in Fig. 1) and at least one memory module (i.e. 130a-n in Fig. 1) having a memory hub (i.e. 140 in Fig. 1) and a plurality of memory devices (i.e. 148 in Fig. 1) coupled to the memory hub, a method of coupling command, address and data signals (i.e. collectively shown as bus 150 in Fig. 1) between the memory hub controller and the memory hub in the at least one memory module (e.g. see paragraphs [0004]-[0005] and Fig. 1), the method comprising:

- coupling command, address and data signals from the memory hub controller to the memory hub in the at least one memory module using a communications path having a first capacity (i.e. using a high-speed "downstream" bus 154 in Fig. 1 having a fixed width, i.e. having a fixed number of conductors) (e.g. see paragraph [0008] and Fig. 1); and
- coupling data signals from the memory hub in the at least one memory module to the memory hub controller using a communications path having a second capacity (i.e. using a high-speed "upstream" bus 156 in Fig. 1 having a fixed width, i.e. having a fixed number of conductors), where the sum of the first capacity and the second capacity is a fixed value (since the first and the second capacities are fixed values, the sum of the first capacity and the second capacity is also a fixed value) (e.g. see paragraph [0008] and Fig. 1).

However, AAPA does not teach about altering the first capacity and the second capacity during the operation of the memory system based on the rate at which the signals are being coupled from the memory hub controller to the memory hub in the at least one memory module and based on the rate at which the signals are being coupled from the memory hub in the at least one memory module to the module memory hub controller. Zhu, on other hand, teaches a system having a dynamic sizing bus controller which controls bus transfers for data transfers between the host device and the slave device such that bus width can have variable width (e.g. see the abstract). Accordingly, it would have been obvious to one of ordinary skills in the art at the time of the current invention was made to implement Zhu's teachings in the memory system disclosed in

AAPA so the logical (i.e. the variable) bus width can be assigned to both communications paths taught by AAPA so the first capacity and the second capacity becomes variable and the sum of them stays constant as claimed. In doing so, the width of both communications paths taught by AAPA can be adjusted as needed based on the rate at which the data is transmitted/received on them. Therefore, the data latency due to the "bottleneck" limiting the data bandwidth in the memory system is avoided.

As per claims 17 and 36, see arguments with respect to the rejection of claim 1. Claims 17 and 36 are also rejected based on the same rationale as the rejection of claim 1.

Regarding claims 3-8, 10-11, 19-26, 28-29, 34, 38-44, 47 and 49-55, the combination of AAPA and Zhu teaches the claimed invention as described above and furthermore, Zhu teaches that the act of altering the first capacity and the second capacity comprise determining the rate at which the selected signals are being coupled and then altering the first capacity and the second capacity at the determined rate (i.e. the slave bus width is automatically configured based on the number of slave cycles generated for the master cycle request) (e.g. see Col. 3, lines 42-47).

As per claims 59-60, 67, 85-86, 91, 97, 102, 105, 119-120, see arguments with respect to rejection of claims 10-11, 28-29, 34, 38-44 and 54-55. Claims 59-60, 67, 85-86, 91, 97, 102, 105, 119-120 are also rejected based on the same rationale as the rejection of claims 10-11, 28-29, 34 and 54-55 as they comprise same limitations as

claims 10-11, 28-29, 34 and 54-55 as indicated by Applicant in Table 2 on page 32 of Remarks.

Regarding claims 9 and 27, the combination of AAPA and Zhu teaches the claimed invention as described above. The further limitation of configuring buffers in the memory hub controller and in the memory hub of at least one memory module as either input buffers or output buffers would be obvious from the Zhu prior art because once the bus width of the input and output buses of the AAPA is adjusted, the buffers also needs to be configured as either input or output buffers accordingly.

Regarding claims 12, 30 and 56, the combination of AAPA and Zhu teaches the claimed invention as described above and furthermore, Zhu teaches that the act of altering the first capacity and the second capacity during the operation of the memory system comprise altering the first capacity and the second capacity within a range of minimum and maximum values for the first capacity and the second capacity respectively (i.e. the slave bus width is automatically configured based on the number of slave cycles generated for the master cycle request) (e.g. see Col. 3, lines 42-47).

As per claims 61, 68, 87 and 121, see arguments with respect to rejection of claims 12, 30 and 56. Claims 61, 68, 87 and 121 are also rejected based on the same rationale as the rejection of claims 12, 30 and 56 as they comprise same limitations as claims 12, 30 and 56 as indicated by Applicant in Table 2 on page 32 of Remarks of the previous response.

As per claim 47, AAPA discloses a processor-based system (i.e. 100 in fig. 1), comprising: a processor (i.e. 104 in Fig. 1) having a processor bus (i.e. 106 in Fig. 1); a

system controller (i.e. 110 in Fig. 1) coupled to the processor bus (i.e. 106 in Fig. 1), the system controller having a peripheral device port (as shown in Fig. 1); and a memory hub controller (i.e. 128 in Fig. 1) coupled to the processor bus, the memory hub controller having an output port and an input port; at least one input device (i.e. 118 in Fig. 1) coupled to the peripheral device port of the system controller; at least one output device (i.e. 120 in Fig. 1) coupled to the peripheral device port of the system controller; at least one data storage device (i.e. 124 in Fig. 1) coupled to the peripheral device port of the system controller; at least one memory module (i.e. 130a-n in Fig. 1) having a memory hub and a plurality of memory devices coupled to the memory hub; a downstream bus (i.e. 154 in Fig. 1) coupled between the output port of the memory controller and the memory hub of the at least one memory module, the downstream bus having a width of M bits (i.e. a fixed width), and an upstream bus (i.e. 156 in Fig. 1) coupled between the input port of the memory controller and the memory hub of the at least one memory module, the upstream bus having a width of N bits where N is equal to a fixed value (i.e. a fixed width), (e.g. see AAPA paragraphs [0004]-[0005], [0007]-[0008] and Fig. 1).

However, AAPA does not teach that N is less than M and N and M are variable. Zhu, on other hand, teaches a system having a dynamic sizing bus controller which controls bus transfers for data transfers between the host device and the slave device such that bus width can have variable width (e.g. see the abstract). Accordingly, it would have been obvious to one of ordinary skills in the art at the time of the current invention was made to implement Zhu's teachings in the memory system disclosed in

AAPA so the logical (i.e. the variable) bus width can be assigned to both communications paths taught by AAPA so the first capacity (i.e. N) and the second capacity (i.e. M) becomes variable and the sum of them stays constant as claimed. In doing so, the width of both communications paths taught by AAPA can be adjusted as needed based on the rate at which the data is transmitted/received on them. Therefore, the data latency due to the "bottleneck" limiting the data bandwidth in the memory system is avoided.

As per claims 58, 66, 73, 78, 82, 84, 93, 99, 104, 107 and 118, see arguments with respect to rejection of claims 1, 9-10, 12-13, 15, 17, 27, 30-31, 33-34, 47 and 53. Claims 58, 66, 73, 78, 82, 84, 93, 99, 104, 107 and 118 are also rejected based on the same rationale as the rejection of claims 1, 9-10, 12-13, 15, 17, 27, 30-31, 33-34, 47 and 53 as they comprise same limitations as claims 1, 9-10, 12-13, 15, 17, 27, 30-31, 33-34, 47 and 53 as indicated by Applicant in Table 1 on page 31 of Remarks of the previous response.

As per claims 16, 35, 37, 46, 57 and 65, the combination of AAPA and Zhu teaches the claimed invention as described above and furthermore, Zhu also teaches the acts of altering the first capacity and the second capacity during the operation of the memory system comprise altering the first capacity and the second capacity during the initialization of the memory system, i.e. the slave bus width is automatically configured based on the number of slave cycles generated for the master cycle request during operation (e.g. see Col. 3, lines 42-47).

As per claims 65, 72, 77, 81, 92, 98, 103, 106, 108, 110 and 122, see arguments with respect to rejection of claims 16 and 35. Claims 65, 72, 77, 81, 92, 98, 103, 106, 108, 110 and 122 are also rejected based on the same rationale as the rejection of claims 16 and 35 as they comprise same limitations as claims 16 and 35 as indicated by Applicant in Table 2 on page 32 of Remarks of the previous response.

As per claims 109-117, see arguments with respect to rejection of claims 37-44 and 46. Claims 109-117 are also rejected based on the same rationale as the rejection of claims 37-44 and 46 as they comprise same limitations as claims 37-44 and 46 as indicated by Applicant in Tables 1-2 on page 31-32 of Remarks of the previous response.

7. Claims 13-14, 31-32, 62-63, 69-70, 74-75, 79, 88-89, 94-95 and 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Zhu, further in view of Hamilton et al. (USPN: 4,443,845) hereinafter, Hamilton.

Regarding claims 13-14 and 31-32, the combination of AAPA and Zhu teaches the claimed invention as described above. However, none of them teaches about the act of altering the first capacity and the second capacity comprise manually altering the first capacity and the second capacity by adjusting at least one electrical connection. Hamilton, on the other hand, teaches about configuring I/O by both manually and automatically using the digital layout programming technique (e.g. see Col. 13, lines 39-42). Accordingly, it would have been obvious to one of ordinary skills in the art at the time of the current invention was made to implement Hamilton's teachings in the

memory system taught by the combination of AAPA and Zhu so the user can adjust the bandwidth of the input/output buses.

As per claims 62-63, 69-70, 74-75, 79, 88-89, 94-95 and 100, see arguments with respect to rejection of claims 13-14 and 31-32. Claims 62-63, 69-70, 74-75, 79, 88-89, 94-95 and 100 are also rejected based on the same rationale as the rejection of claims 13-14 and 31-32 as they comprise same limitations as claims 13-14 and 31-32 as indicated by Applicant in Table 2 on page 32 of Remarks of the previous response.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hetul Patel whose telephone number is 571-272-4184. The examiner can normally be reached on 8:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

H.B Patel 04/05/07

Hetul Patel
Patent Examiner
Art Unit 2186